Claims

1. (Original) A manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region and an active region, electrically isolated by the element isolation region, on a semiconductor layer; and

(b) forming a resistive impurity layer, at least, in a part of the active region by forming a first impurity-doping region, and providing a first impurity-doping forbidden region in the element isolation region at the same time.

2. (Currently Amended) The manufacturing method of the semiconductor device according to [[the]] claim 1, wherein a plurality of the resistive impurity layers are formed, and the first impurity-doping forbidden region is formed so as to isolate [[, at least]] the adjacent first impurity-doping regions in the (b).

3. (Currently Amended) The manufacturing method of the semiconductor device according to [[the ]] claim 1 or claim 2, further comprising;

[[(c)]] forming a contact impurity layer by forming a second impurity-doping region in a region, continuously connected to the resistive impurity layer.

4. (Currently Amended) The manufacturing method of the semiconductor device according to [[the ]] claim 3, wherein a second impurity-doping forbidden region is provided, at least, in the element isolation region when forming the second impurity-doping region [[in the (c)]].

5. (Currently Amended) The manufacturing method of the semiconductor device according to [[the ]] claim 4, wherein a plurality of the contact impurity layers are formed, and the second impurity-doping forbidden region is formed so as to isolate, at least, the adjacent second impurity-doping regions [[in the (c)]].

6. (Original) A manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region and an active region, electrically isolated by the element isolation region, on a semiconductor layer;

(b) forming a resistive impurity layer, at least, in a part of the active region by forming a first impurity-doping region; and

(c) forming a contact impurity layer by forming a second impurity-doping region in a region, continuously connected to the resistive impurity layer, and providing a second impurity-doping forbidden region, at least, in the element isolation region at the same time.

7. (Currently Amended) The manufacturing method of the semiconductor device according to [[the ]] claim 6, wherein a plurality of the contact impurity layers are formed, and the second impurity-doping forbidden region is formed so as to isolate, at least, the adjacent second impurity-doping regions [[in the (c)]].

8. (Original) A manufacturing method of a semiconductor device, in which a resistive impurity layer formed in an active region, and an insulation gate type heavy insulated transistor and an insulation gate type light insulated transistor having different drain-source breakdown voltages, are integrated on a same semiconductor layer, comprising:

(a) forming an element isolation region and an active region, electrically isolated by the element isolation region, on the semiconductor layer;

(b) forming an insulation layer above the semiconductor layer;

(c) forming a resistive impurity layer, at least, in a part of the active region by forming a first impurity-doping region in a forming region for the resistive impurity layer, and providing a first impurity-doping forbidden region in the element isolation region at the same time;

(d) forming a gate insulation layer of the heavy insulated transistor in a forming region for the heavy insulated transistor by patterning the insulation layer to a predetermined shape, and removing the insulation layer in forming regions for the light insulated transistor and the resistive impurity layer;

(e) forming a gate insulation layer of the light insulated transistor in the forming region for the light insulated transistor;

(f) forming a gate conductive layer of the each transistor on the first gate insulation layer and the second gate insulation layer; and

(g) forming a source/drain region of the each transistor by doping a second impurity.

9. (Currently Amended) The manufacturing method of the semiconductor device according to [[the ]] claim 8, wherein the source/drain region of the each transistor is formed by doping the second impurity, and a contact impurity layer is formed in a region, continuously connected to the resistive impurity layer, in the forming region for the resistive impurity layer [[in the (g)]].

10. (Currently Amended) The manufacturing method of the semiconductor device according to [[the]] claim 9, wherein a second impurity-doping region is provided, at least, in the active region in the forming region for the resistive impurity layer when doping the second impurity, and a second impurity-doping forbidden region is provided, at least, in the element isolation region [[in the (g)]].

11. (Currently Amended) The manufacturing method of the semiconductor device according to [[the]] claim 10, wherein a plurality of the contact impurity layers are formed, and the second impurity-doping forbidden region is formed so as to isolate, at least, the adjacent second impurity-doping regions [[in the (g)]].

12. (Currently Amended) The manufacturing method of the semiconductor device according to any of [[the]] claims 9 through 11, wherein a plurality of the resistive impurity layers are formed, and the first impurity-doping forbidden region is formed so as to isolate, at least, the adjacent first impurity-doping regions [[in the (c)]].

13 (Original) A manufacturing method of a semiconductor device, in which a

resistive impurity layer formed in an active region, and an insulation gate type heavy insulated transistor and an insulation gate type light insulated transistor having different drain-source breakdown voltages, are integrated on a same semiconductor layer, comprising:

(a) forming an element isolation region and an active region, electrically isolated by the element isolation region, on the semiconductor layer;

(b) forming an insulation layer above the semiconductor layer;

(c) forming a resistive impurity layer, at least, in a part of the active region by forming a first impurity-doping region;

(d) forming a gate insulation layer of the heavy insulated transistor in a forming region for the heavy insulated transistor by patterning the insulation layer to a predetermined shape, and removing the insulation layer in forming regions for the light insulated transistor and the resistive impurity layer;

(e) forming a gate insulation layer of the light insulated transistor in the forming region for the light insulated transistor;

(f) forming a gate conductive layer of the each transistor on the first gate insulation layer and the second gate insulation layer; and

(g) forming a source/drain region of the each transistor by doping a second impurity, as well as forming a contact impurity layer in a region, continuously connected to the resistive impurity layer, and providing a second impurity-doping forbidden region, at least, in the element isolation region at the same time.

14. (Currently Amended) The manufacturing method of the semiconductor device according to [[the]] claim 13, wherein a second impurity-doping region is provided, at least, in the active region in the forming region for the resistive impurity layer when doping the second impurity, and a second impurity-doping forbidden region is provided, at least, in the element isolation region [[in the (g)]].

15. (Currently Amended) The manufacturing method of the semiconductor device according to [[the]] claim 14, wherein a plurality of the contact impurity layers are

formed, and the second impurity-doping forbidden region is formed so as to isolate, at least, the adjacent second impurity-doping regions [[in the (g)]].

16. (Currently Amended) The manufacturing method of the semiconductor device according to any one of the claims 1, 2, 4 through 8, or 12 through 15, wherein the element isolation region is semi-recessed LOCOS.

17. (Original) A semiconductor device, comprising:

a semiconductor layer;

an insulation gate type heavy insulated transistor and an insulation gate type light insulated transistor having different drain-source breakdown voltages and formed on the semiconductor layer; and

a resistive impurity layer formed on the semiconductor layer.

18. (Currently Amended) The semiconductor device according to [[the]] claim 17, wherein an element isolation region and an active region, electrically isolated by the element isolation region, are formed on the semiconductor layer, and the resistive impurity layer is formed in the active region.

19. (Currently Amended) The semiconductor device according to [[the]] claim 17 or claim 18, wherein the element isolation region is semi-recessed LOCOS.

20. (New) The method as in claim 1, wherein the resistive impurity layer is formed by one of doping an n-type impurity, and doping a p-type impurity.

21. (New) The method of claim 13, wherein a thickness of a gate insulation layer of said heavy insulated transistor is thicker than a gate insulation layer of said light insulated transistor.

22. (New) The method of claim 3, wherein said contact impurity layer has a higher concentration of impurity than said resistive impurity layer.